

## CHAPTER 3

### BASIC APPLICATIONS CIRCUITS FOR CMOS DACs OPERATED IN THE CONVENTIONAL CURRENT-STEERING MODE

#### 3.1 UNIPOLAR (CURRENT-STEERING)

Figure 3.1 shows the conventional unipolar D/A converter connection for CMOS DACs. Resistors R1 and R2 are used to trim out any gain error. Resistor R2 places the error band in a region which permits correction within the range of adjustment of R1. For the higher resolution applications (10 bits and up) R1 and R2 should be precision resistors with matched temperature coefficients, as their temperature coefficients can become significant in terms of overall circuit performance. If possible, R1 should be a fixed resistor, rather than a potentiometer, and its value is selected at the time of system calibration. The appropriate value of R2 may be calculated according to the equation.

$$R2 = \frac{(\text{Max DAC Gain Error in } \%) \cdot (RDAC_{\text{max}})}{100}$$

$RDAC_{\text{max}}$  is the specified maximum input resistance of the DAC. At the reference terminal the maximum range of resistance for R1, when R1 is a potentiometer, may be calculated according to the equation

$$R1 = 2 \cdot R2$$

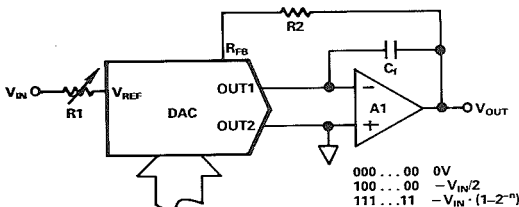


Figure 3.1 Unipolar D/A Converter (Current Steering)

Some CMOS DACs guarantee a maximum gain error of  $\pm 1\text{LSB}$  which may eliminate the requirement for gain error adjustment. Capacitor  $C_f$  is for phase compensation and is usually 39pF (see Section 2.4.1). If the op amp is stable when configured with the DAC,  $C_f$  may be omitted in applications where settling time or overshoot is unimportant. Input bias current compensation resistors, normally connected to the positive input of the op amp, should not be used, as bias currents can give rise to a voltage offset which in turn results in errors due to the noise gain of the DAC, (see 2.4.2).

The advantages of this particular circuit are its simplicity and low component count. The input impedance presented to  $V_{REF}$  is constant, and  $V_{IN}$  can exceed the supply voltage ( $V_{DD}$ ) to the DAC. The main disadvantage of the circuit is that it requires a reference voltage opposite in polarity to the output voltage; as a result single supply operation is not possible.

#### 3.2 OP AMPS FOR CURRENT-STEERING MODE DACs<sup>(5)</sup>

The primary requirement for the current-steering mode is an amplifier with low input bias currents and low input offset voltage. The input offset voltage of an op amp is multiplied by the variable "noise gain", (see Section 2-4-2) of the circuit. A change in noise gain between two adjacent digital fractions produces a step change in the output voltage due to the amplifier's input offset voltage. This output voltage change is superimposed upon the desired change in output between the two codes and gives rise to a differential linearity error. If the product of the amplifier input offset voltage and the incremental change in noise gain between adjacent codes exceeds

– 1LSB, a “perfect” D/A converter will nevertheless be non-monotonic. The worst-case incremental changes in noise gain occur on the steps from (Mid-range – 1LSB) to Mid-range and from Mid-range to (Mid-range + 1LSB)—see Figure 2-10. It should be noted that in audio circuits even a small amount of offset can cause an audible “thump” at the output when the DAC changes code.

The input bias current of an op amp also generates an offset at the voltage output as a result of the bias current flowing in the feedback resistor  $R_{FB}$ . Most op amps have input bias currents low enough to prevent any significant errors (100nA gives an error of about 0.5mV) but the user is cautioned to note that the input bias currents of some JFET amplifiers do reach significant levels at high temperature.

FET-input amplifiers, with low input offset voltage specifications, such as AD542, exhibit negligible offset error due to bias current and are therefore normally used as DAC output amplifiers. For wide temperature range or precision circuits, superbeta input amplifiers such as AD517 work well. They do not have as good a slew rate as the JFET amplifiers, but their open-loop gain is higher and the input offset and bias currents are much lower over the operating temperature range. As a rule of thumb, the maximum input offset voltage for an op amp should be less than 0.1LSB bit weight. For example, a 12-bit DAC with 0 to 10V output range has an LSB bit weight of approximately 2.4mV, which dictates a maximum input offset voltage of less than 240μV. Amplifiers with higher specified offsets can be used if the offset is nulled in-circuit using the external offset trim facilities of the op amp. However, the need to maintain low offset over temperature, the additional cost of an offset trim potentiometer, and the labor to do the calibration is usually much greater than buying the appropriate op amp in the first place. Figure 3.2 shows a method of nulling offset for op amps which do not have external correction terminals. The trimmer is adjusted until OUT1 (not  $V_{OUT}$ ) is at zero volts and therefore the same potential as OUT2.

The overall settling time of the circuit is a complex function determined by circuit capacitance, gain-bandwidth product of the output amplifier (GBW) and the amplifiers slew rate. For a simple guideline, it is useful to note that the small signal settling time observes the following relationship:

$$\text{Small signal settling time} \propto \sqrt{\frac{R_{FB}(C_O + C_F)}{2 \times \text{GBW}}}$$

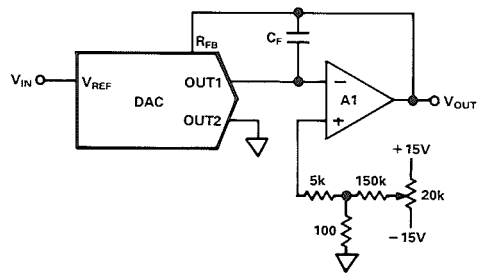


Figure 3.2 Alternative Method of Nulling Op Amp Offset

For optimal settling time in the current-steering mode, DAC output capacitance must be as low as possible and the unity gain-bandwidth product as high as possible.

Finite op amp gain also affects the DAC static accuracy. For example, in the simple D/A converter circuit shown in Figure 3.1.

$$V_{OUT} = -D \cdot V_{IN} \left[ \frac{1}{1 + \frac{1}{A} [\text{Noise Gain}]} \right]$$

Thus, the gain-dependent error is approximately

$$D \cdot V_{IN} \cdot \frac{1}{A} \cdot [\text{Noise Gain}]$$

where  $D$  is the fractional binary code  $A$  is the open loop gain of the amplifier and the “Noise Gain” is the variable gain due to variable output resistance of the DAC. For a 12 bit converter, the value of noise gain at full scale is about 2.0 (See Section 2.4.2).

The error due to finite open loop gain of the amplifier should not be greater than 0.1 LSB. This translates into gains of 5,000, 20,000 and 80,000 for 8-, 10- and 12-bit converters respectively. Fortunately most op amps meet this requirement easily although some of the lower cost (e.g., LM324) or very high speed op amps (e.g., LH0032) do not have adequate gain particularly for 12-bit applications.

### 3.3 BIPOLAR OUTPUT (OFFSET BINARY AND 2’S COMPLEMENT CODING)

The circuit of Figure 3.1 can be modified to give bipolar output by biasing the overall gain negative and doubling the DAC gain as shown in the circuit of Figure 3.3. A code of all 0’s corresponds to negative full scale (i.e.,  $-V_{IN}$ ) all 1’s code gives full scale i.e.,  $V_{IN}(1-2^{-(n-1)})$ . If an inverter is inserted in the MSB line (shown dotted) then the circuit responds to 2’s complement coding.

$R_1$ ,  $R_2$  and  $R_3$ , should be precision metal film or

wire-wound resistors with matching temperature coefficients. Potentiometers may be used for R1 and R3; however the temperature coefficients of potentiometers vary with position and are unlikely to match R2. In practice, R1 and R3 are best made up

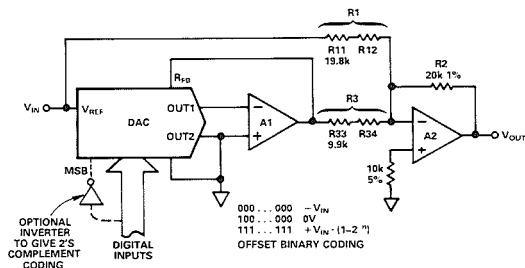


Figure 3.3 Bipolar Output D/A Converter

of two resistors in series as shown. R11 and R33 are slightly less than the correct values for R1 and R3 and then R12 and R34 are small value resistors selected at calibration to make up the appropriate value. The circuit is calibrated as follows: first, negative full scale is applied to the digital inputs (all 0's at the DAC), and R12 is selected to give  $-V_{IN}$  at the output. Then positive full scale is applied (all 1's at the DAC) and R34 is selected to give  $V_{IN}(1-2^{-(n-1)})$  at the output. A calibration check is then made for zero volts out (1,000...000 at the DAC). The value of R33 + R34 must compensate not only for tolerance errors in R2, but also for gain error in the D/A converter. The value of R33 is therefore given by:

$$R33 = \frac{R2}{2} \frac{(1 - \text{Max \% Gain Error} - R2\% \text{ Tolerance})}{100}$$

The main advantages of this circuit are simplicity, constant reference input impedance, and that  $V_{IN}$  can exceed the DAC supply voltage.

The main disadvantages are the two-point calibration procedures required and that one bit of resolution is effectively lost in providing the sign—i.e., the 12-bit resolution spans from negative full scale to positive full scale, resulting in 11-bit resolution for each half-scale.

### 3.4 BIOPOLAR OUTPUT (SIGN + MAGNITUDE CODING)

Figure 3.4 shows a CMOS DAC connected for sign plus magnitude coding. It is similar to the circuit of Figure 3.1 except that the VREF input is switched between  $+V_{IN}$  and  $-V_{IN}$ , depending on the sign bit. Amplifier A2 buffers the VREF input so that variations in the on-resistance of the CMOS switch do not affect calibration.  $+V_{IN}$  and  $-V_{IN}$  are often

available together within a system; but where they are not both present, one can be generated from the other by a simple inverter circuit. The advantage of Figure 3.4 circuit is that it has only a single point calibration for gain error (unlike the circuit of Figure 3.3 which has a two point calibration).

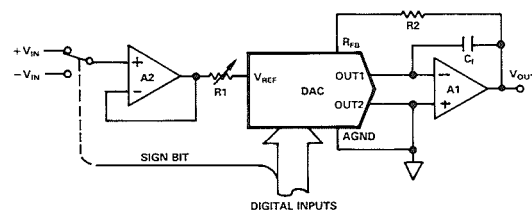


Figure 3.4 Sign Plus Magnitude D/A Converter

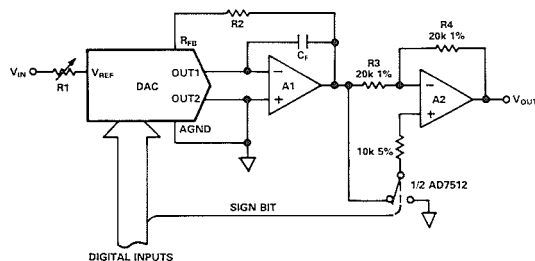


Figure 3.5 Alternative Sign Plus Magnitude D/A Converter

Figure 3.5 shows an alternative circuit for sign plus magnitude coding. This circuit does not require positive and negative reference voltages, but it does require an additional output op amp. Two point calibration is made by first adjusting R3 until the output has equal magnitude for positive and negative full scale and then R1 is adjusted to give the correct full scale. In any system using more than one DAC the circuit of Figure 3.4 is to be preferred since the input buffer op amp A2 minimizes loading on the reference source and the circuit requires fewer components. The input resistance of CMOS DACs (typically 10 kilohms) is quite low—where many DACs are used, they can easily overload the reference source.

### 3.5 SINGLE SUPPLY DAC WITH OFFSET SCALE

One solution to the design of D/A converters with an offset scale is shown in Figure 3.6. The DAC is operated in the conventional current-steering mode but with OUT2 (and hence OUT1) biased positive by an

amount  $V_{BIAS}$ . For this circuit to operate correctly, the ladder termination resistor must be connected to OUT2. The output voltage is given by:

$$V_{OUT} = \left\{ D \cdot \frac{R_{FB}}{RDAC} \cdot (V_{BIAS} - V_{IN}) \right\} + V_{BIAS}$$

Thus from  $D = 0$  to  $D = 1-2^{-n}$  the output voltage varies from  $V_{OUT} = V_{BIAS}$  to approximately  $2V_{BIAS} - V_{IN}$ .

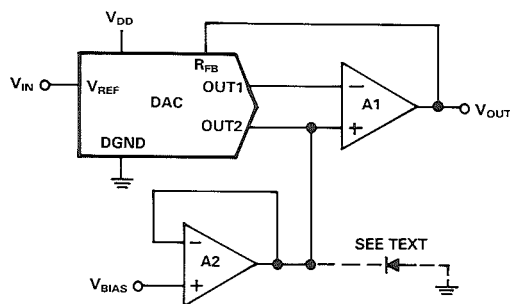


Figure 3.6 Single Supply D/A Converter with Scale Offset from Zero (Current-Steering)

This circuit is useful in that it operates from a single supply voltage with  $V_{BIAS}$  positive. It also maintains the full multiplying capability of the DAC.  $V_{IN}$  can go outside the supply rails without damaging the circuit.  $V_{BIAS}$  should be a low impedance source capable of sinking (or sourcing) all possible variations in current at the OUT2 terminal without any problems. Other schemes for operating CMOS DACs from a single supply voltage are discussed in Chapter 4. If this circuit is used with dual power supplies, positive and negative, it is possible that on power-up the op amp supplying  $V_{BIAS}$  may exhibit a transient negative voltage at its output, possibly creating heavy currents which might damage the circuit. To protect against this, include a diode as shown dotted in Figure 3.6. Practical circuits using this method are given in Figures 6.2.4. and 6.5.9.

### 3.6 CHANGING THE GAIN OF CMOS DACs<sup>(4)</sup>

Sometimes the DAC output voltage range is required to be greater than  $V_{IN}$ . For example, a DAC may be required to operate with a system reference of  $-5V$ , but deliver a 0 to  $+10V$  output (i.e., gain of  $-2$ ). The gain could be achieved in an external amplifier stage. It can also be achieved in a single stage. However, in situations such as this, it is important to study the effect of the temperature coefficients of the thin-film resistors that are used to make up the DAC.

At first sight, the gain of a CMOS DAC could be increased by adding a resistor,  $R_2$ , in series with the feedback resistor, or it could be reduced by adding a resistor  $R_1$  in series with  $V_{REF}$  as shown in Figure 3.7. This is the method used to trim out gain error as described in Section 3-1. However, for significant changes in gain,  $R_1$  or  $R_2$  will be large relative to the DAC resistors and the temperature coefficients of  $R_1$  and  $R_2$  are unlikely to match the resistor temperature coefficient of the DAC (typically  $-300\text{ppm}/^\circ\text{C}$ ). As a result, the circuit displays a very large gain temperature coefficient. To overcome this problem, the circuit of Figure 3.8 is recommended where gains greater than 1 are required.  $R_1$ ,  $R_2$  and  $R_3$  should all have similar temperature coefficients but they need not match the temperature coefficient of the DAC. Gain is best adjusted by varying the attenuator ratio, as adjustment sensitivity is almost unaffected by  $R_3$ .

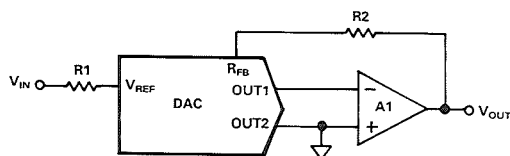


Figure 3.7 Wrong Method of Changing Gain of Current-Steering D/A Converter

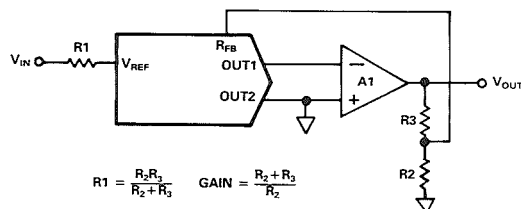


Figure 3.8 Correct Method of Increasing Gain of Current-Steering D/A Converter

### 3.7 VOLTAGE REFERENCES

Most references are specified with a given temperature coefficient in terms of  $\text{ppm}/^\circ\text{C}$ . The reference temperature coefficient should be consistent with the system accuracy specifications. For example, an 8-bit system required to hold its overall specification to within 1LSB over the temperature range  $0-50^\circ\text{C}$  dictates that the maximum system drift with temperature should be less than  $78\text{ppm}/^\circ\text{C}$ . A 12-bit system for the same temperature range requires a maximum drift of  $5\text{ppm}/^\circ\text{C}$  and if the temperature range is increased to  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  then the maximum tolerable system drift is  $1.4\text{ppm}/^\circ\text{C}$ . These figures apply for a total change of 1LSB from the minimum

to maximum temperature. In practice, the maximum permissible drift with temperature is often stated for temperature variations about an ambient temperature of 25°C and the maximum change with temperature may then be relaxed accordingly.

The lowest cost reference circuits are temperature compensated zeners, and bandgap references which synthesize a reference voltage based on the bandgap voltage of silicon (1.23V). Bandgap references such as AD589 are low cost but their output voltage usually has to be buffered to the appropriate level. It is important to consider the offset voltage drift of the op amp when using a buffer amplifier. A drift trimmed op amp, such as AD547, which has been manufactured, trimmed and tested for low drift and offset should be used for the buffer op amp. Alternatively, use a buffered bandgap reference such as the AD584. It is trimmed at the wafer stage to deliver 2.5V, 5V, 7.5V or 10V outputs.

Temperature compensated zeners offer an alternative method of generating a reference voltage. Generally, the reference zener is constructed as a sub-surface zener so that it has lower noise and better stability than the conventional surface zener. The typical

temperature drift of a zener is 30 to 50ppm/°C with selections down to 10ppm/°C. Zener references can be further improved, either by incorporating them with an on-chip heater, which keeps the reference temperature constant or by utilizing them in a trimmed hybrid circuit which corrects for second order errors and allows drifts down to 1ppm/°C to be achieved. The on-chip heater method of stabilizing the reference voltage is used in the LM399 family. It is an effective way of protecting against temperature drift but consumes about 20mA of current. The output voltage of the LM399 is nominally 6.95 volts and usually requires an output buffer amp. The AD2710 series of references also use buried zener references but their temperature stability of 1ppm/°C is achieved by the use of active circuitry and active laser trimming. They deliver 10 volt outputs without the requirement for an external buffer amplifier.

For high resolution applications (14 bits and above), the user is cautioned to study the output noise characteristics of the circuit reference since reference noise can contribute significant errors. Buried zener type references usually have lower noise than bandgap references.

